UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,688	07/15/2003	Eiji Natori	110405.01	7058

25944 7590 11/02/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
WILSON, CHRISTIAN D	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,688	NATORI ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/931,915.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07152003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano *et al.*

Regarding claim 1, Hirano *et al.* (US 6,163,043) discloses a method of fabricating a memory cell array formed of ferroelectric capacitors in a matrix [Figure 1] comprising the steps of forming a first signal electrode **111a** with a pattern **D1** on a base **101**, selectively forming a ferroelectric layer **113** linearly along the first signal electrode, and forming a second signal electrode **112a** in a direction **D2** intersecting the first signal electrode.

Regarding claims 6 and 7, Hirano *et al.* discloses a dielectric layer **104** between the laminates of the first signal electrode and ferroelectric layer which covers the exposed surface of the base [Figure 2] and is formed of a material having a dielectric constant lower than the dielectric constant of the ferroelectric layer [column 10, lines 18-30].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano *et al.* in view of Clem *et al.*

Hirano *et al.* teaches a method of fabricating a memory cell array as described above, but discusses an etching method instead of a selective formation method. Clem *et al.* (US 6,518,168) teaches a fabrication method of a ferroelectric memory comprising the steps of forming a base with a first region **22** having a surface which provides improved adhesion for the first electrode layer and a second region **20** which provides poor adhesion for the first electrode layer [column 5, lines 55-67], and selectively forming the first signal electrode in the first region. Clem *et al.* further teaches the first and second regions defined on the surface of the base [Figures 1a – 1d], and exposing the surface of the base in the first region and forming a forming an undercoat **20** with a low affinity for materials of the first signal electrode and ferroelectric layer [Figure 1d]. Also, Clem *et al.* teaches exposing the base in the second region and forming an undercoat layer in the first region with a high affinity for materials of the first signal electrode and ferroelectric layer [Figures 2a – 2c]. It would have been obvious to one of ordinary skill in the art to use the patterning methods of Clem *et al.* in the method of Hirano *et al.* since Clem *et al.* teaches that the use of a blocking agent with chemical vapor deposition reduces fabrication costs and reduces chemical process waste [column 2, lines 22-30].

5. Claims 8 – 12 and 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano *et al.* in view of Yoo.

Regarding claim 8, Hirano *et al.* teaches a method of fabricating a memory cell array formed of ferroelectric capacitors in a matrix [Figure 1] comprising the steps of forming a first signal electrode **111a** with a pattern **D1** on a base **101**, selectively forming a ferroelectric layer **113** linearly along the first signal electrode, and forming a second signal electrode **112a** in a direction **D2** intersecting the first signal electrode. Hirano *et al.* does not discuss forming the ferroelectric layer linearly along the second signal electrode and intersecting the first signal electrode. Yoo (US 6,077,716) teaches the formation of the ferroelectric layer linearly with the second signal electrode [Figure 22a] and intersecting the first signal electrode [Figure 22b]. It would have been obvious to one of ordinary skill in the art to use the method of Yoo in the method of Hirano *et al.* since Yoo teaches that this method provides heightened integration and improved productivity [column 10, lines 5-15].

Regarding claim 9, Yoo further teaches etching the second signal electrode and ferroelectric layer with the same mask. It would have been obvious to one of ordinary skill in the art to use the etching method of Yoo in the method of Hirano *et al.* since Yoo teaches that using the same mask reduces the number of processing steps [column 10, lines 19-25].

Regarding claims 10 and 11, Hirano *et al.* discloses a dielectric layer **104** between the laminates of the second signal electrode and ferroelectric layer which covers the exposed surface of the base and the first signal electrode [Figure 2] and is formed of a material having a dielectric constant lower than the dielectric constant of the ferroelectric layer [column 10, lines 18-30].

Regarding claim 12, Hirano *et al.* teaches a method of fabricating a memory cell array formed of ferroelectric capacitors in a matrix [Figure 1] comprising the steps of forming a first signal electrode **111a** with a pattern **D1** on a base **101**, selectively forming a ferroelectric layer **113** linearly along the first signal electrode, and forming a second signal electrode **112a** in a direction **D2** intersecting the first signal electrode. Hirano *et al.* does not discuss forming patterning the ferroelectric layer so that it is only disposed at the intersection of the first and second electrodes. Yoo (US 6,077,716) teaches patterning the ferroelectric layer so that it is only disposed at the intersection of the first and second electrodes [Figure 22b]. It would have been obvious to one of ordinary skill in the art to use the method of Yoo in the method of Hirano *et al.* since Yoo teaches that this method provides heightened integration and improved productivity [column 10, lines 5-15].

Regarding claim 17, Yoo further teaches etching the second signal electrode and ferroelectric layer with the same mask. It would have been obvious to one of ordinary skill in the art to use the etching method of Yoo in the method of Hirano *et al.* since Yoo teaches that using the same mask reduces the number of processing steps [column 10, lines 19-25].

Regarding claims 18 – 20, Hirano *et al.* discloses a dielectric layer **104** between the laminates of the first signal electrode and ferroelectric layer which covers the exposed surface of the base and the first signal electrode [Figure 2] and is formed of a material having a dielectric constant lower than the dielectric constant of the ferroelectric layer [column 10, lines 18-30].

6. Claims 13 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano *et al.* and Yoo as applied to claim 12 above, and further in view of Clem *et al.*

Hirano *et al.* as modified by Yoo teaches a method of fabricating a memory cell array as described above, but discusses an etching method instead of a selective formation method. Clem *et al.* teaches a fabrication method of a ferroelectric memory comprising the steps of forming a base with a first region **22** having a surface which provides improved adhesion for the first electrode layer and a second region **20** which provides poor adhesion for the first electrode layer [column 5, lines 55-67], and selectively forming the first signal electrode in the first region. Clem *et al.* further teaches the first and second regions defined on the surface of the base [Figures 1a – 1d], and exposing the surface of the base in the first region and forming a forming an undercoat **20** with a low affinity for materials of the first signal electrode and ferroelectric layer [Figure 1d]. Also, Clem *et al.* teaches exposing the base in the second region and forming an undercoat layer in the first region with a high affinity for materials of the first signal electrode and ferroelectric layer [Figures 2a – 2c]. It would have been obvious to one of ordinary skill in the art to use the patterning methods of Clem *et al.* in the method of Hirano *et al.* since Clem *et al.* teaches that the use of a blocking agent with chemical vapor deposition reduces fabrication costs and reduces chemical process waste [column 2, lines 22-30].

Conclusion

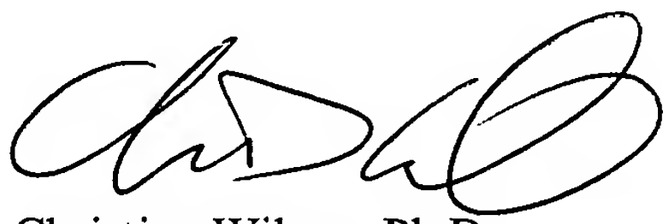
7. A copy of the search history (EAST and STN) is enclosed.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art teaches methods of forming a matrix of ferroelectric memory cells.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2824

CDW